GRA & AFCH

DDS 9912 Arduino Shield

V1.x

OPERATING INSTRUCTION

Firmware v. 1.01

Rev. A

Use only a power supply with a voltage rating of 7.5 volts or USB to power this device!

GENERAL GUIDE

The device is an expansion board (shield) for Arduino **Mega** based on the ATmega2560 microcontroller with 5-volt logic levels, since the board has logic signal level converters from 5V to 3.3V.

Power is supplied to the device through the Arduino, and connection is made either through the power jack (up to 7.5 volts) or through the USB connector.

To fully operate the device, an I²C OLED display of 0.96 inches is required (optional and not included). The display is powered by 5 volts from the 5V Pin on the Arduino.

The device is controlled by an encoder and a BACK button (not used in the current software version). An external encoder and pushbutton can be connected to the **ExENC** (PH2.0-3p) and **ExBACK1** (PH2.0-2p) connectors, if needed. The AD9912 clocking can be done in three ways:

5-volt USB power input

7.5-volt power input

Figure 1

- Crystal;
- OCXO/TCXO (default);
- From an external source, when using it, **make sure that capacitor C20 is removed** (Figure 2), **and resistor PLL_BP 1 kOhm is installed.** To achieve the best results, refer to Table 1.

The type and frequency of the clock source must be correctly set in the device settings. All settings are saved in non-volatile memory.

The device has 3 outputs types: **Sinus**, **CMOS** and **Differential HSTL**. The output signal of the **Sinus** channel is taken from the SMA connector labeled "**RF OUT**", the output signal of the **CMOS** channel is taken from the "**CMOS**" connector, and the output signals of the **HSTL** channel are taken from the "**HSTL A**" and "**HSTL B**" connectors.
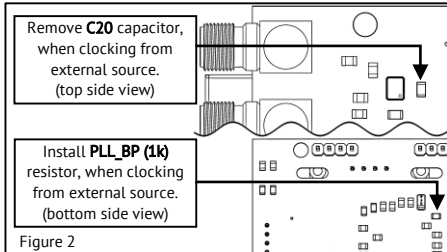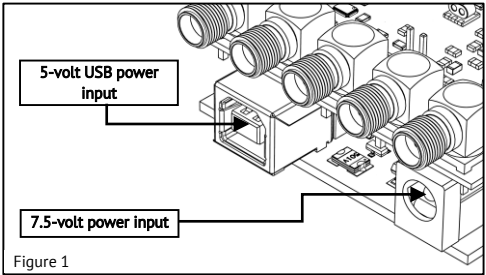

Remove **C20** capacitor, when clocking from external source. (top side view)

Install **PLL_BP (1k)** resistor, when clocking from external source. (bottom side view)

Figure 2

Output RF Transformer

Low-pass RF Filter 600 MHz

REF CLK IN
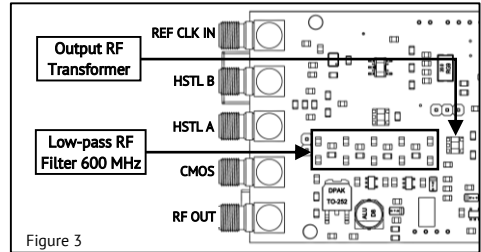
HSTL B

HSTL A

CMOS

RF OUT

Figure 3

When using an **external clock source**, the signal is fed to the SMA connector labeled "**REF CLK IN**", when using it, **make sure that capacitor C20 is removed** (Figure 2), **and resistor PLL_BP 1 kOhm is installed.** To achieve the best results, refer to Table 1.

The device contains an output low-pass filter and a matching output transformer, therefore a software **limit of 100 kHz** is applied to the minimum output frequency of the device (Figure 3).

OPERATION

Rotating the encoder knob moves the cursor through menu items or changes the value of the selected item. Pressing the encoder knob activates or deactivates the parameter editing mode, or enters a submenu (depending on the context). Fast rotation of the knob allows jumping through 10 values at a time.

The frequencies at the HSTL and CMOS outputs are tied to the Sinus channel (RF OUT), but the frequency at the HSTL output can be **multiplied** by 2, and the frequency at the CMOS output can be **divided** by a divider ranging from 1 to 65535.

Main menu:

RFsin: sets the frequency at the output of the Sinus channel (RF OUT). The maximum output frequency is limited to 500 MHz, but it is important to note that the maximum output frequency that can be obtained is AD9912 core frequency x 0.4. For example, with a core frequency of 1 GHz, the maximum output frequency cannot exceed 400 MHz. The core frequency can be changed in the "Setup" menu. For proper operation of the Sinus channel, the 'CMOS/HSTL ENABLE' jumper must be **OPEN**. If it is not removed, the level at the 'RF OUT' output will be reduced by 3dBm!

HSTL: Enables or disables the signal at the HSTL outputs and, and allows doubling the frequency on this channel, in addition to software configuration, the "CMOS/HSTL ENABLE" jumper must be **CLOSED**. The voltage on the outputs is switched by the "REF LEVEL" jumper and can be either **1.8V** or **3.3V**. The frequency range on this output is 100 kHz to 1 GHz.

CMOS: Enables or disables the signal at the CMOS output, in addition to software configuration, the "CMOS/HSTL ENABLE" jumper must be **CLOSED**. The frequency range on this output is 1 Hz to 500 MHz.

DIV: This option is only available when the CMOS channel is enabled. It sets the frequency divider for the CMOS channel in the range from 1 to 65535.

dBm: The signal level at Sinus channel (RF OUT) can be adjusted from -7 dBm to +4 dBm.

Sweep menu - "Sweep":

Pressing the encoder knob when the "Sweep" item is selected will bring up the frequency "Sweep" menu. Changes to the parameters take effect only after the "START" option is activated, and at this moment, all parameter values are saved in non-volatile memory. After activating the Sweep mode, the "START" menu item changes to "STOP", and control of the device is blocked until the encoder knob is pressed or the set time elapses (for a single pass mode).

From: set the initial frequency within the range of 100 kHz to 500 MHz with step sizes of 1 Hz.

To: set the initial frequency within the range of 100 kHz to 500 MHz with step sizes of 1 Hz.

Sec, mSec: sets the time for the frequency to change from the "From" value to the "To" value. This parameter can take values from 1 to 999, and the units can be selected from "Sec" for seconds and "mSec" for milliseconds.

↑↓: the frequency will change first from a "FROM" value to a "TO" value, and then in the reverse direction. This mode is also known as **NO-DWELL HIGH** (or **NO-DWELL LOW**, if "TO" value lower than "From" value). The total time to complete one frequency cycle from the starting value to the ending value and back to the starting value will be twice as long as the time set in the previous menu item.

↑: the frequency will change only from a "FROM" value to a "TO" value, after which it will stop at the final frequency value (if the infinity mode was not enabled).

⟳: the number of frequency change cycles will be **infinite**, which means that as soon as one cycle is completed, a new one will begin immediately. The only way to stop the frequency change is by pressing the encoder knob. If the **NO-DWELL** mode is activated, the frequency will change in both directions during each cycle: from the starting value to the ending value, and then back. If the **NO-DWELL** mode is not activated, each cycle will start with a frequency jump to the starting value.

1: the frequency change will stop at the end of one cycle (if the **NO-DWELL** mode was enabled, then the frequency will smoothly return to the starting value).

Setup menu:

To enter the setup menu, press and hold the "MODE" button for 1 second.

Clock Src: Allows selecting the clock source, with three options available: "XO AT-cut" - Crystal Oscillator, "TCXO/OCXO" - Temperature Compensated Crystal Oscillator / Oven-Controlled Crystal Oscillator, "REF CLK IN" - External clock source. In addition to selecting the clock source in the menu, it is also necessary to ensure that the components listed in the Table 1 are set to the position corresponding to the selected clock source.

Clock source (only one at a time)	Capacitors				Resistors				Ferrite Bead
	C20	C18, C19	C14, C17	C15	XO	REF	PLL_BP(1k)	R37	FB1
XO - Crystal Oscillator (Z1)	–	✔	✘	✔	✔	✘	✘	✔	✘
TCXO - Oscillator 1ppm (Z2)	✘	✘	✔	✔	✘	✔	✘	✔	✔
OCXO - Oscillator 0.1ppm (Z3)	✘	✘	✔	✔	✘	✔	✘	✔	✔
REF CLK IN - External Generator	✘	✘	✔	✘	✘	✔	✔	✘	✘

Table 1

✔ means that the component must be installed,

✘ means that the component must be removed,

– means it doesn't matter.

Clock Freq: Allows setting the frequency of the clock source, with different frequencies available for each source:
- For "XO", frequencies of 20 MHz and 25 MHz are available;
- For "TCXO/OCXO", frequencies of 10, 20, 25, 40, and 50 MHz are available;
- For "REF CLK IN", it is possible to manually set the frequency in the range of 250 MHz to 1500 MHz, a step of 1 MHz.

Src Doubler: enabling this option reduces the level of phase noise but increases the level of sub-harmonics. This option is not available if an external clock source "REF CLK IN" is selected.

DDS Core Clock: Allows changing the core frequency. When clocked by "XO" or "TCXO/OCXO", the core frequency can be set from 700 MHz to 1300 MHz, with the adjustment step depending on the clock source frequency. When clocked by an external source, the core frequency can be set in the range of 250 MHz to 1500 MHz (by setting the clock source). The nominal AD9912 core frequency is 1000 MHz, setting a higher frequency is overclocking, and operation is not guaranteed.

The clock settings are applied only after selecting the "**SAVE**" option.

⚠ **WARNING**	**It is not recommended to set the core frequency above 1200 MHz**

| RF OUT Frequency:	100 kHz – 400 MHz (500* MHz) in 1 Hz step
Spurs max:	-60 dBc
Frequency step:	1 Hz
Output power:	-7 dBm to +4 dBm (on 50 Ohm load)
Output level up to:	1 Vpeak-to-peak (at +4 dBm)
Power Supply:	USB or External Power Supply DC 7.5V, 1A
Output filter:	9-th order, 600 MHz cut-off
CMOS Frequency:	1 Hz to 250 MHz
HSTL Frequency:	100 kHz to 800 MHz (1000* MHz)
HSTL Output Level:	1.8 V or 3.3 V
Reference clock sources (on choice):	XO-Crystal Oscillator, TCXO 1ppm, OCXO 0.1ppm, External Oscillator 250 - 1500 MHz
Reference clock input level (REF CLK IN)	0 dBm - +10 dBm, 0.632 – 2 Vpp
Size:	53.2 x 105 x 50 mm

Figure 4
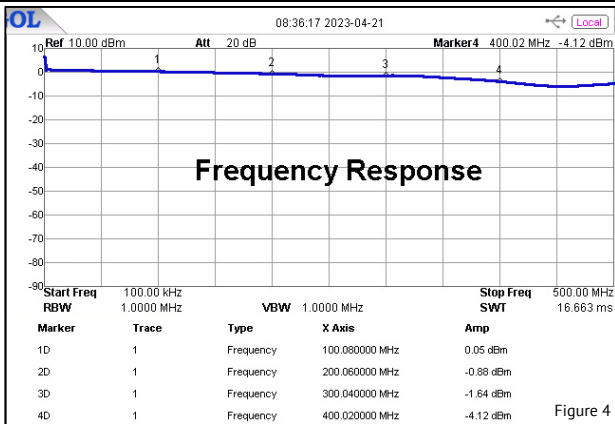
FACTORY RESET

To reset all settings to factory defaults, you should hold down the "Mode" button and apply power to the device while keeping the button pressed.

REMOVING 100 KHz MINIMUM FREQUENCY LIMIT

For experienced users only. All actions are performed at your own risk. Remove transformer T1 and replace it with one capacitor and two resistors (Figure 5), and in the file "DDS-AD9912-Firmware.ino" set the desired value in Hertz in the line `#define LOW_FREQ_LIMIT 100000`. Installing a capacitor C1_1 with a value of 10 uF will reduce the lower frequency limit to 10 Hz, if you want to reduce the limit even more, then the value of the capacitor should be increased. These modifications will lead to a degradation in the performance of the DDS: the output level will decrease by 3 dBm, and the level of harmonics will increase as the current mirror and a balanced transformer not be used.

Figure 5
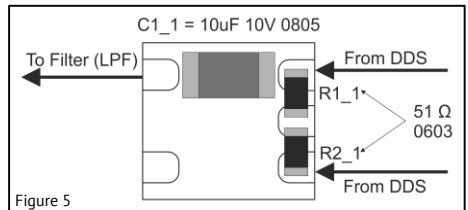
website:
www.gra-afch.com

firmware:
www.github.com/afch/DDS-AD9912-Arduino-Shield

video compilation of firmware:
youtu.be/Zn1xLlvlVXE