

# DDS9959 Arduino Shield

V1.1

4 Synchronized Channels  
(Independent Freq/Phase/Amplitude)

**OPERATING MANUAL**

Firmware v1.23

## ⚠ WARNING

Use only a power supply with a voltage rating of 7.5 volts or USB-port to power this device!

## GENERAL GUIDE

The device is an expansion board (shield) for Arduino Mega based on the ATmega2560 microcontroller with **5-volt** logic levels, since the board has logic signal level converters from **3.3V to 5V**.

Power is supplied to the device through the Arduino, and connection is made through the power jack (**7.5 volts only!**) or through the USB connector.

To fully operate the device, an **I<sup>2</sup>C OLED display of 1.3 inches** is required (optional and not included). The display is powered by **5 volts** from the **5v pin** on the Arduino.

The device is controlled by an **encoder** and a **BACK** button. An **external encoder** and **push-button** can be connected to the **ExENC** (PH2.0-3p) and **ExBACK** (PH2.0-2p) connectors, if needed.

The **AD9959 clocking** can be done in **three** ways:

- Using **On Board XO** Crystal source;
- Using **On Board TCXO** source;
- Using an external source (TCXO/OCXO/Oscillator (Generator) with output impedance **50 Ohm**), when using it,

**make sure that capacitor C20 (100nF 0805) is removed** (Figure 2). This will **disconnect** on board TCXO **output** from **DDS Clk input**.

The type and frequency of the clock source **must be correctly set** in the device settings (At "**SETUP**" menu). All settings are saved in non-volatile memory.

The **output signals** is taken from the **SMA** connectors labeled "**RF OUTx**" on the board.

When using an **external clock source**, the signal is fed to the **SMA** connector labeled "**REF CLK IN**", when using it, **make sure that capacitor C20 is removed** (Figure 2).

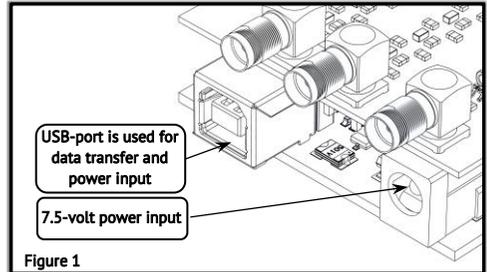


Figure 1

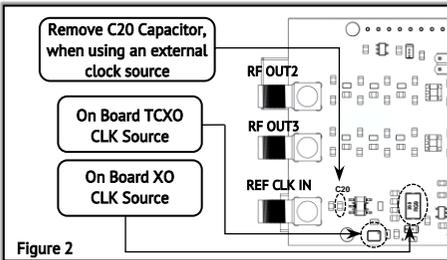


Figure 2

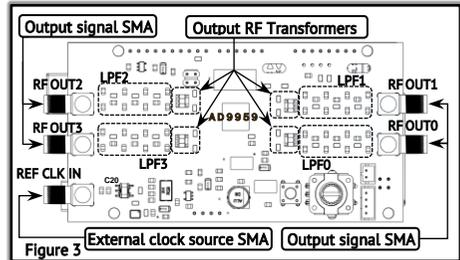


Figure 3

The level of the external clock signal **must be** within the range of **0 dBm to +10 dBm** for a sinusoidal signal. For example, if the signal level from an external generator is **+16 dBm**, it is necessary to connect it only through an attenuator of at least **6 dB (16 dBm - 6 dB = 10 dBm)**. For signals of other waveforms, such as a clipped sine or square wave, the level must be **0.4 - 2 Vpp**.

The device contains a **low-pass filter** and an output **matching transformer** on each of the **four outputs (RF OUT 0-3)**, therefore a software limit of **100 kHz** is applied to the minimum **output frequency** of the device (Figure 3).

## OPERATION

After powering on the module, **firmware** information is displayed on the screen for 2 seconds.

Notifications are displayed in the "**Info string**" area. For example, it may indicate that the set frequency value exceeds the allowable limit.

Hint:	Ch	Freq.Hz	dBm	Phase
Push and hold Encoder to enter Setup.	F0	144.000.000	-10	000.0°
	F1	144.000.000	-15	090.0°
	F2	144.000.000	-24	270.0°
	F3	072.000.000	-18	120.0°
Firmware ver.: 1.23	Information Area GR&AFCH			

## Main menu:

Rotating the **encoder knob** moves the cursor through menu items or changes the value of the selected item. **Pressing** the encoder knob activates or deactivates the parameter editing mode, or enters a submenu (depending on the context). Fast rotation of the knob allows jumping through **10** values at a time.

**Channel selection:** Before changing the parameters, select the channel in the first column of the main menu table.

**Frequency [Hz]:** The maximum **output frequency** is limited to **40%** of the frequency of the AD9959 core. For example, with a core frequency of **500 MHz**, the maximum output frequency **cannot exceed 200 MHz**. The **core frequency** can be changed in the **"Setup"** menu.

**Amplitude: [dBm]** The signal level can be adjusted from **-60 dBm** to **-7 dBm**.

**Phase  $\varphi$ : [deg]** The phase shift value can be adjusted from **0.0°** to **360.0°** with **0.1°** degrees step.

To return to the channel selection column, click the **"Back"** button.

Ch	Freq. [Hz]	dBm	Phase [°]
F0	144.000.000	-10	000.0°
F1	144.000.000	-15	090.0°
F2	144.000.000	-24	270.0°
F3	072.000.000	-18	120.0°

Ch	Freq. [Hz]	dBm	Phase [°]
F0	144.000.000	-10	000.0°
F1	144.000.000	-15	090.0°
F2	144.000.000	-24	270.0°
F3	072.000.000	-18	120.0°

## Setup menu: (To enter the settings menu, *press and hold* the encoder knob for 2 second)

**Clock Src:** Allows selecting the **Software clock source**, with **two** options available:

- "TCXO/OCXO"** - Temperature Compensated Crystal Oscillator / Oven-Controlled Crystal Oscillator. In this case, DDS PLL is **enabled** and the **hardware** clock sources can be the **On Board TCXO** or External **OCXO/TCXO** connected to **"REF CLK IN"** input via SMA connector.
- "External clock"** - In this case, DDS PLL is **disabled**, and **hardware** clock sources are an **External Generator** connected to **"REF CLK IN"** input via SMA connector **ONLY**.

In addition to selecting the clock source in the menu, it is also necessary to ensure that the component listed in the **Table 1** are set to the position corresponding to the **hardware** clock source.

SETUP	
Clock Src:	TCXO/OCXO
Clock Freq:	50 MHz
Core Clock	500 MHz
SAVE	EXIT

SETUP	
Clock Src:	Ext. Clock
Clock Freq:	500 MHz
Core Clock	500 MHz
SAVE	EXIT

Clock source (only one at a time)	Capacitors			Resistors	
	C20	C18, C19	C14, C17	XO	REF
On Board XO - Crystal 20ppm (Z1)	*	✓	*	✓	*
On Board TCXO - Oscillator 1ppm (Z2)	✓	*	✓	*	✓
REF CLK IN - External Generator or OCXO or TCXO	*	*	✓	*	✓

**Table 1.**

✓ means that the component must be installed, \* means that the component must be removed,

**Clock Freq:** Allows setting the frequency of the clock source, with different frequencies available for each source:

- For **"TCXO/OCXO"**, frequencies of **25, 40, 50, 100** and **125 MHz** are available (**50 MHz** on default). **PLL is enabled**;
- For **"External clock"**, it is possible to manually set the frequency in the range of **400 MHz** to **600 MHz** (depend by Model, refer to Specification) with a step of **1 MHz**. **PLL is disabled**.

SETUP	
Clock Src:	Ext. Clock
Clock Freq:	500 MHz
Core Clock	500 MHz
SAVE	EXIT

SETUP	
Clock Src:	TCXO/OCXO
Clock Freq:	50 MHz
Core Clock	500 MHz
SAVE	EXIT

**DDS Core Clock:** Allows changing the core frequency. When in "Clock Src." the **"TCXO/OCXO"** option is selected and PLL is **enabled**, the core frequency can be set from **400 MHz** to **600 MHz**, with the adjustment step depending on the clock source frequency. When in "Clock Src." the **"Ext. Clock"** option is selected and PLL is **disabled**, the core frequency can be set in the range of **400 MHz** to **600 MHz** with step **1 MHz**. The nominal AD9959 core frequency is **600 MHz**, setting a **higher** frequency is **overclocking**, and operation at such a frequency is **not guaranteed!!!**

The clock settings are **applied only after** selecting the **"SAVE"** option. The **"EXIT"** option allows exiting **without saving** the settings.

### ⚠ WARNING

**It is not recommended to set the core frequency above 600 MHz!**

**Factory Reset:** To **reset** all settings to **factory defaults**, you should **hold down** the encoder knob and **apply power** to the device while keeping the button pressed.

**Communication Interface:** Starting with version **1.21**, the ability to control via the serial port has been added. To view the list of serial port commands, **follow** the link below (**QR firmware**).

# SPECIFICATIONS

OUTPUTS TYPES (SMA):	4 Synchronized Channels (Independent Freq/Phase/Amplitude); Impedance: 50Ω
REFERENCE CLOCK INPUT (SMA):	0.4 to 2 $V_{peak-to-peak}$ , 0 dBm to +10 dBm; Impedance: 50Ω
FREQUENCY RANGE:	100 kHz to 225 MHz @500 MHz Core Clock, with 1 Hz frequency step
FLATNESS:	±2.5dB from 100kHz to 225MHz, full scale (referred to Figure 4)
SPECTRAL PURITY:	Spurious: <-50dBc below 200MHz / Harmonic: <-50dBc below 200MHz
PHASE $\Phi$ STEP:	0.0° to 360.0° with 0.1° degrees step
OUTPUT POWER:	-7 dBm to -60 dBm (on 50 Ohm load)
OUTPUT LEVEL UP TO:	0.28 $V_{peak-to-peak}$ (-7 dBm 50 Ohm at 100 MHz) *Refer to Figure 4.
POWER SUPPLY:	By USB or External Power Supply DC 7.5V, 1A
OUTPUT FILTER:	7-th order, 240 MHz cut-off (-3 dB)
ON BOARD REFERENCE CLOCK SOURCES (ON CHOICE):	TCXO 50 MHz 1ppm Oscillator (default), XO 25 MHz 20ppm Oscillator (alternative) or External Oscillator up to 600 MHz (if using built-in PLL then DDS clock is limited to 600MHz)
DISPLAY (ON CHOICE):	OLED 1.3 inches 1°C
SIZE:	53 x 115 x 47 mm (W x L x H)
WEIGHT:	46 g (without Arduino and display) / 105 g (with Arduino and display)

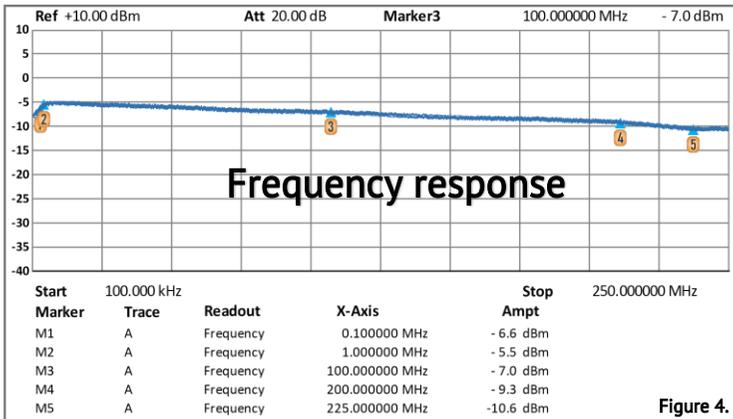


Figure 4.

## Lowering the minimum output frequency limit from 100kHz to 10Hz, for AD9959

**For experienced users only.** All actions are performed at your own risk. Remove transformer **T1** and replace it with one capacitor and two resistors (Figure 5), and in the file "DDS-AD9959-Arduino-Shield.ino" set the desired value in Hertz in the line `#define LOW_FREQ_LIMIT 100000`. Installing a capacitor **C1\_1** with a value of **10 uF** will reduce the lower frequency limit to **10 Hz**. If you want to reduce the limit even more, then the value of the capacitor should be increased. These modifications will lead to a degradation in the performance of the DDS: the output level will decrease by **3 dBm**, and the level of harmonics will increase as the current mirror and a balanced transformer not be used.

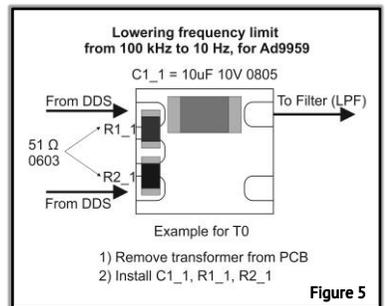


Figure 5



Website:

[www.gra-afch.com](http://www.gra-afch.com)



Video Tutorial:

[youtu.be/HpiqOwic9mg](https://youtu.be/HpiqOwic9mg)



Firmware:

[github.com/afch/DDS-AD9959-Arduino-Shield](https://github.com/afch/DDS-AD9959-Arduino-Shield)



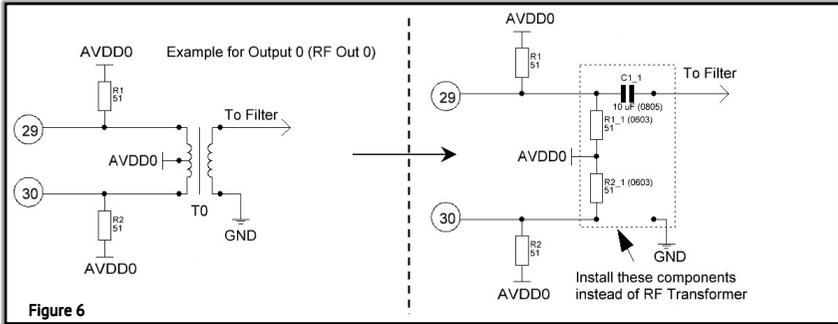
Video compilation of firmware:

[youtu.be/3RPriA\\_Rh4](https://youtu.be/3RPriA_Rh4)

# Appendix

## Lowering the minimum output frequency limit from 100kHz to 10Hz, for AD9959

The diagram shows changes in the electrical schematic to reduce the minimum operating frequency of the output signal (see Figure 6):



## List of Serial Port Commands:

Starting with version **1.21**, the ability to control via the serial port has been added.

- C** – Set the current output Channel: (0 – 3)
- F** – Sets Frequency in Hz (100000 – 225000000)
- A** – Sets the power (Amplitude) level of the selected channel in dBm (-60 – -7)
- P** – Sets the Phase of the selected channel in dBm (0 – 360)
- M** – Gets Model
- E** - Enable Outputs (ALL)
- D** - Disable Outputs (ALL)
- V** – Gets Firmware Version
- h** – This Help
- ;** – Commands Separator

Example: **C0;F100000;A-10**

Sets the Frequency to **100** kHz, and Output Power (Amplitude) to **-10** dBm on Channel **0** (**RF OUT0**). Any number of commands in any order is allowed, but the very first command must be **"C"**

**Serial Port Settings:** Speed - 115200 Bouds, **Data Bits** – 8, **Stop Bits** – 1, **Parity** – No, **DTR** – OFF.

### Windows:

An example of setting up a serial port in the Windows console:

```
mode COM3 baud=115200 DTR=OFF Data=8
```

Usage example:

```
echo F100000000 > COM3
```

### Ubuntu 22.04:

An example of setting up a serial port in the Ubuntu:

```
sudo usermod -aG dialout $USER_NAME$
sudo chmod a+rw /dev/ttyUSB0
sudo stty -F /dev/ttyUSB0 115200 cs8 ixoff -hupcl -
echo
```

Usage example:

```
echo "F100000000" > /dev/ttyUSB0
```